DATA SHEET

SAA7346
Shock absorbing RAM addresser

Preliminary specification
File under Integrated Circuits, IC01

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Philips Semiconductors

PHILIPS

Shock absorbing RAM addresser SAA7346

FEATURES

- Absorbs shocks from x, y and z directions
- Absorbs rotational shocks
- Absorbs multiple shocks per second
- Interfaces directly to compact disc decoders SAA7345, SAA7347 and SAA7370
- Multi-speed I^2S-bus input with single-speed I^2S-bus output
- Controls 1 or 4 MBit of external Dynamic Random Access Memory (DRAM)
- Easy serial interface for communication with common microcontrollers
- Software selectable shock detectors
- By-pass/power-down mode
- Kill interface for DAC deactivation
- Can be used for:
  - ‘sampling’ part of a disc
  - to reduce access pauses between jumps
  - to deliver a programmable delay
  - to generate a fixed audio rate from Constant Angular Velocity (CAV) discs.

GENERAL DESCRIPTION

The SAA7346 can be used to make a CD player insensitive to shocks. To do this, SAA7346 operates closely with a standard 1 Mbit or 4 Mbit DRAM. Audio data is stored inside the DRAM and during shocks the data of the DRAM can be played. The SAA7346 functions as a customized DRAM controller with serial I/O and on-board shock detectors.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	3.3	5.0	5.5	V
I_{DD}	supply current	–	12	–	mA
f_{clk}	clock frequency	–	16.9344	–	MHz
$f_{i(clk)}$	I^2S input word clock frequency	44.1	88.2	176.4	kHz
$f_{o(clk)}$	I^2S output word clock frequency	44.1	88.2	176.4	kHz
T_{amb}	operating ambient temperature	–40	–	+85	°C
T_{stg}	storage temperature	–65	–	+150	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7346H	44	QFP(1)	plastic	SOT307-2

Note

1. When using reflow soldering it is recommended that the Dry Packing instructions in the *“Quality Reference Pocketbook”* are followed. The pocketbook can be ordered using the code 9398 510 34011.

BLOCK DIAGRAM

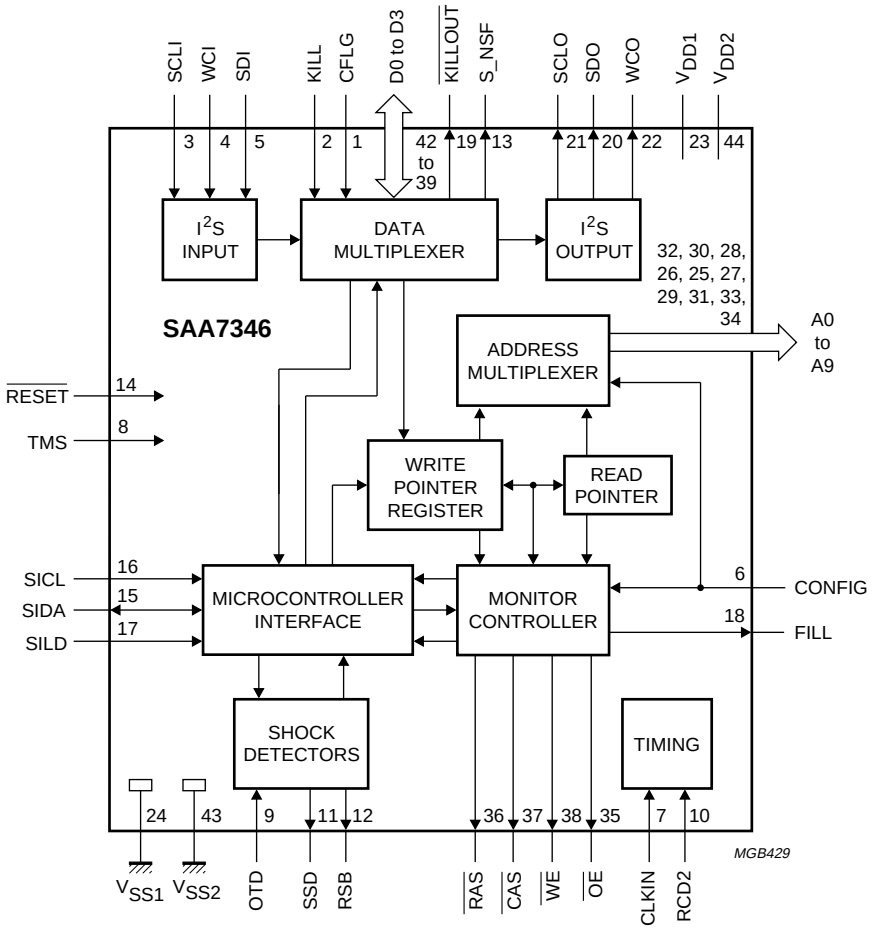


Fig.1 Simplified SAA7347 block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CFLG	1	correction flag input from CD decoder
KILL	2	kill input
SCLI	3	multi-speed I^2S bit clock input
WCI	4	multi-speed I^2S word clock input
SDI	5	multi-speed I^2S data input
CONFIG	6	external DRAM select input; HIGH 4 Mbit, LOW 1 Mbit
CLKIN	7	16.9344 MHz system clock input
TMS	8	test mode select input; active HIGH
OTD	9	on/off track detector input
RCD2	10	DRAM read cycle divide-by-2 input; active HIGH
SSD	11	shock detected output; active HIGH when shock is detected
RSB	12	rotational shock busy output; active HIGH when rotational shock is detected
S_NSF	13	synthetic new subcode frame output
$\overline{\text{RESET}}$	14	reset enable input; active LOW
SIDA	15	microcontroller interface input/output data line
SICL	16	microcontroller interface clock input
SILD	17	microcontroller interface $\overline{\text{read}}$/write input
FILL	18	FIFO write enable output; active HIGH
$\overline{\text{KILLOUT}}$	19	open drain output; active LOW; when in by-pass mode $\overline{\text{KILLOUT}}$ equals KILL
SDO	20	I^2S data output
SCLO	21	I^2S bit clock output
WCO	22	I^2S word clock output
V_{DD1}	23	supply voltage 1
V_{SS1}	24	supply ground 1
A4	25	DRAM address bus output 4
A3	26	DRAM address bus output 3
A5	27	DRAM address bus output 5
A2	28	DRAM address bus output 2
A6	29	DRAM address bus output 6
A1	30	DRAM address bus output 1
A7	31	DRAM address bus output 7
A0	32	DRAM address bus output 0
A8	33	DRAM address bus output 8
A9	34	DRAM address bus output 9
$\overline{\text{OE}}$	35	DRAM enable output; active LOW
$\overline{\text{RAS}}$	36	DRAM row address strobe output; active LOW
$\overline{\text{CAS}}$	37	DRAM column address strobe output; active LOW
$\overline{\text{WE}}$	38	DRAM write enable output; active LOW

SYMBOL	PIN	DESCRIPTION
D3 to D0	39 to 42	DRAM data bus inputs/outputs
V_{SS2}	43	supply ground 2
V_{DD2}	44	supply voltage 2

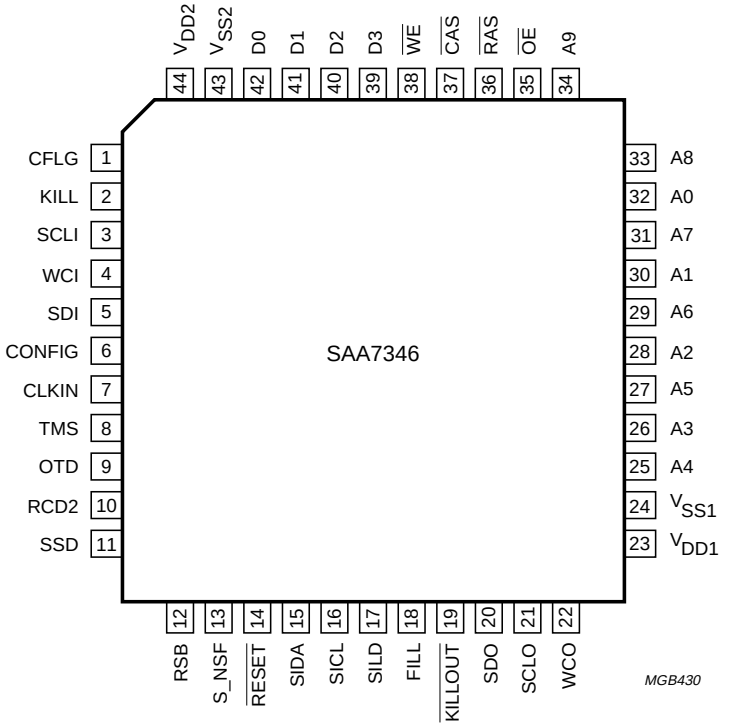


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

I²S input/output interfaces

The SAA7346 contains an asynchronous serial input and a serial output interface. The serial operation of the interfaces is under hardware control of the external circuitry and uses the I²S protocol. The output presents a continuous clock signal SCLO (typically 2.8224 MHz) which is divided from the system clock, and a word select signal WCO, typically 44.1 kHz (f_s), which is used to distinguish between right and left channels. When in by-pass mode WCO and SCLO are the same as the input interface signals WCI and SCLI, enabling data to pass through the SAA7346. Since the serial input port is asynchronous the device is independent of the CD decoder clock speed and enables the word clock to vary from $1.1 \times f_s$ to $4 \times f_s$ (typically $2 \times f_s$). This is a requirement of any electronic shock absorbing system since the disc must be rotating faster than usual to assure the FIFO is full to absorb a shock. The falling edge of WCO indicates the start of a new transfer. Data is exchanged over the SDI and SDO pins. The SAA7346 is compatible with a variety of DAC ICs.

New subcode frame regeneration

The SAA7346 has a digital phase-locked loop (PLL) system which decodes the F1 and F6 flags, from the first 1-bit signal generated by the CD decoder correction flag output shown in Fig.3. The F1 flag is the absolute time sync signal of the New Subcode Frame (NSF). It relates

the position of the subcode-sync to the audio data. This signal determines the accuracy with which the SAA7346 sews audio data together after a shock. When the CD decoder preforms a jump the NSF will be missed. The PLL system will insert the missing pulse. The resulting signal is the S_NSF which can be used as a time out for reading the subcode from the decoder shown in Fig.4. The S_NSF is available externally and the NSF flag can be read via the serial microcontroller interface. The F6 flag indicates at least one hold has occurred in the decoder's error corrector and interpolator. The shock processor uses this signal to evaluate whether a shock has occurred.

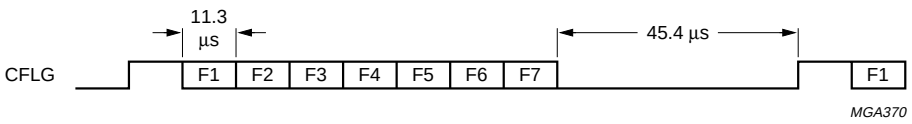


Fig.3 CFLG input timing diagram.

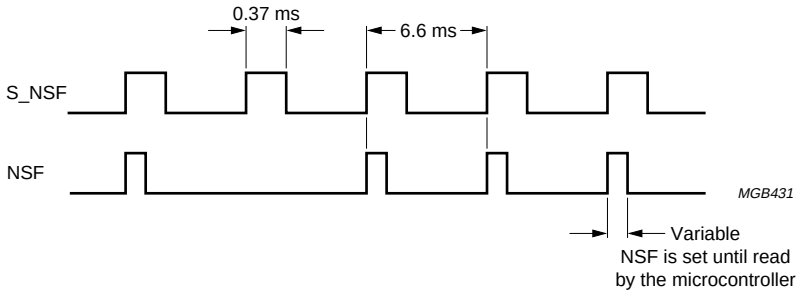


Fig.4 S_NSF output timing diagram; n = 2.

Shock processor

The shock processor determines whether a shock has occurred by processing all the shock detectors. The SAA7346 will enter shock mode and set SSD when the:

- µCsd flag is set by the microcontroller in the command register
- OTD input is active while the jmp_bz flag is not set
- RSB output is set while the e_rot_sd flag is set
- NSF pulse is lost and the full flag is not read by the microcontroller from the status register.

When the target position has been found the microcontroller should set the PFB flag in the command register. The SAA7346 will respond by clearing the SSD flag and start refilling. If CFLG still indicates a hold, the decoder is rolling out of its FIFO. RSB will be set which sets SSD again thus the FIFO will not start refilling. The microcontroller should jump one track back and look for the correct target position again. When the motor speed is stable and the decoder does not roll out of its FIFO, the audio data will be glued together.

SSD will be reset whenever the microcontroller sets PFB or the flush flags in the command register, or when the FIFO empties while the echo flag is LOW. Note if the microcontroller wants SSD to be clear for a while the shock detectors should be inhibited.

FIFO controller and monitor

The SAA7346 uses a state machine to control and monitor the conditions of the FIFO shown in Fig.5.

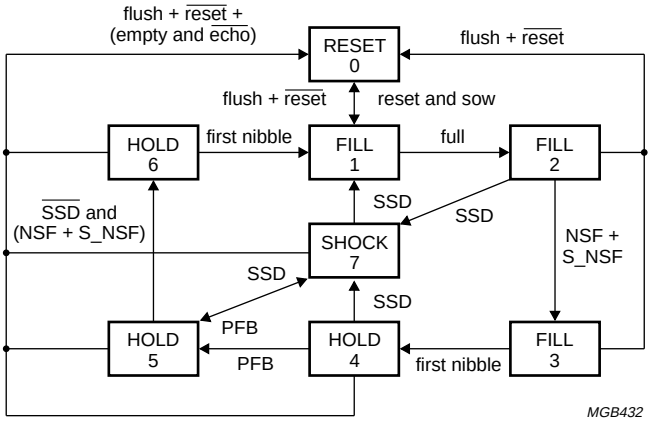


Fig.5 State machine flow diagram.

During normal operation the FIFO will fill up because writing is carried out twice as fast as reading; this is the fill mode. If the FIFO is full the monitor will detect and set the full flag. At the same time the fill flag will be reset thus preventing audio data from being written in to the FIFO. When the microcontroller reads the full flag from the status register, the servo control should jump back one track. The microcontroller enters a wait loop until the same absolute time subcode frame turns by again; this is the hold mode. When the spot is found again the microcontroller should set the PFB flag in the command register and the SAA7346 will resume writing to the DRAM. While in fill mode the write pointer address is saved at the end of each subcode frame. When the player exists hold mode it restores the saved address and continues writing after the last sample.

When a shock is detected the SAA7346 will enter shock mode. The shock mode will last until the PFB is set by the microcontroller or the FIFO is flushed, reset or runs empty.

Microcontroller interface

The SAA7346 has a 3-line microcontroller interface which is compatible with TDA1301, TDA1303 and SAA7345.

Writing data to the SAA7346

The SAA7346 command register is shown in Table 1. This can be written to via the microcontroller interface as shown in Fig.6. The command register flags functions are shown in Table 2.

Table 1 SAA7346 microcontroller interface registers.

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Command	flush	bypass	echo	jmp_bz	otd_p	e_rot_sd	µCsd	PFB
Status	Lm	Lm1	FRM_ER	NSF	full	empty	SSD	fill

Table 2 Command register flag functions.

COMMAND	DESCRIPTION
Flush	Flush, when set, will empty the FIFO, reset the read and write pointer addresses. Then writing will resume to the FIFO. Flag reset automatically.
Bypass	Bypass, when set, will power down the SAA7346. The I^2S interface passes input to output directly. The parallel interface port controls $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{OE}$ which are pulled HIGH. KILL passes directly to $\overline{KILLOUT}$. When exiting by-pass mode the FIFO is automatically flushed.
Echo	Echo, when set, will cause the FIFO contents to be continuously played until the correct position is found again.
jmp_bz	Jump busy, when set, indicates a jump is being preformed. The OTD shock detector input will be disabled. After the jump has finished the flag should be reset by a write.
otd_p	OTD polarity enable. Enables the polarity of the OTD input to be switched from active HIGH set, active LOW not set.
e_rot_sd	Enable rotational shock detection, when set, will detect shocks whenever the decoder rolls out of its internal FIFO.
µCsd	Microcontroller shock detected is set when the microcontroller has detected a shock.
PFB	Position Found Back, when set, indicates that the microcontroller has found the absolute time frame after a shock or hold cycle. The audio data will sew together and the flag reset automatically.

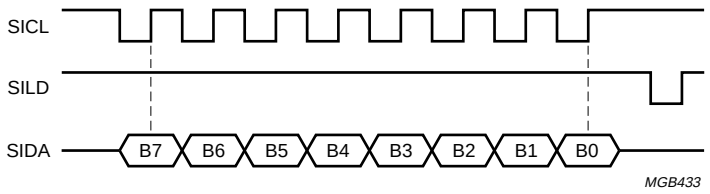


Fig.6 Microcontroller WRITE timing.

Writing operation sequence:

- SILD is held HIGH by the microcontroller.
- Microcontroller data is clocked into the internal command register on the LOW-to-HIGH clock transition of SICL.
- SILD is pulled LOW by the microcontroller to latch-in data to the command register.
- SICL and SILD are pulled HIGH by the microcontroller to indicate that communications have finished.

READING STATUS OF SAA7346

The SAA7346 has a status register shown in Table 1. This can be read via the microcontroller interface shown in Fig.7. The internal status signals are made available on the SIDA pin and are shown in Table 3.

Table 3 Internal status signals.

STATUS	DESCRIPTION
Lm and Lm1	The two Most Significant Bits (MSB) of the FIFO. These can be used to display the FIFO length or correct the subcode time information. The FIFO length is shown in Table 4.
FRM_ER	Framing error flag is set when: 1. The microcontroller did not accept the previous subcode flag on time. When this occurs the NSF flag will be set together with FRM_ER. 2. The S_NSF generated signal does not coincide with the NSF signal generated by the decoder. When this occurs there has been a FIFO overflow in the decoder or a jump. Framing error flag is reset when status register is read.
NSF	New subcode frame is set when an absolute sync is recovered from the CFLG input. Reset when status register is read. If the NSF is still set at the next occurrence of a subcode frame, FRM_ER will be set indicating that the microcontroller has lost a frame.
Full	Full is set when the FIFO is full. When the flag is set the microcontroller must jump back to the previous track. Reset when status register is read.
Empty	Empty is set when the FIFO is emptied during hold or shock modes. DRAM writing should resume immediately unless echo is set in the command register. If set, writing can only resume when PFB or flush are set in the command register. The latter will cause a discontinuity in music. Note when set there is a complete word left in the FIFO giving the SAA7346 controller time to switch to fill mode.
SSD	Set shock detect is set when SAA7346 detects a shock.
Fill	Fill is set when writing data to the DRAM or by setting the command register flags PFB or flush. Reset internally when full or SSD are set.

Table 4 FIFO length as a function of CONFIG, Lm and Lm1.

CONFIG	Lm	Lm1	FIFO LENGTH (s)
0	0	0	0.00 to 0.19
0	0	1	0.19 to 0.39
0	1	0	0.39 to 0.58
0	1	1	0.58 to 0.78
1	0	0	0.00 to 0.75
1	0	1	0.75 to 1.50
1	1	0	1.50 to 2.25
1	1	1	2.25 to 2.97

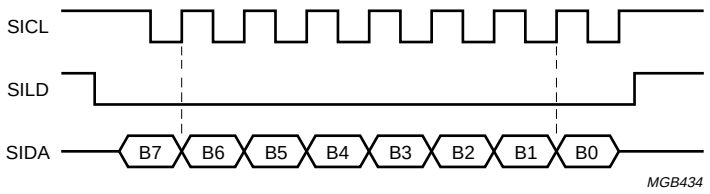


Fig.7 Microcontroller READ timing.

Read operation sequence:

- SILD is held LOW by the microcontroller.
- Status information is clocked from the internal status register on the LOW-to-HIGH clock transition of SICL.
- SICL and SILD are pulled HIGH by the microcontroller to indicate that communications have finished.

DRAM interface

The SAA7346 may be connected to all standard 80 ns, 1M × 4 bit or 256K × 4 bit fast page mode DRAMs. The best performance can be expected with the 4 Mbit DRAM. The CONFIG input selects the DRAM configuration either HIGH 4 Mbit or LOW 1 Mbit format. The SAA7346 converts audio data from serial to parallel and stores it as 4 bits. The addresses for read or write actions are calculated by separate read and write pointers which are multiplexed onto a 4 bits address bus. The control signal outputs associated with the parallel inputs/outputs are shown in Table 5.

Table 5 Command register flag functions.

COMMAND	DESCRIPTION
$\overline{WE}$	indicates write enable action
$\overline{RAS}$	row address strobe
$\overline{CAS}$	column address strobe
$\overline{OE}$	output buffer enable for external memory during cycle.

When the SAA7346 leaves bypass mode where all parallel Port control lines are pulled HIGH, the device initiates a DRAM power-up routine in accordance with the JEDEC standard.

System clock

The system clock input, CLKIN, recommended input signal is 16.9344 MHz. The accuracy of this clock influences the accuracy of the I^2S output, therefore the performance of the DAC and hence audio quality. The system clock is divided by 384 to derive the I^2S output word clock, WCO divided by 8 to derive the I^2S output bit clock, SCLO. Therefore whatever clock jitter the user introduces on the CLKIN signal will be reflected in the WCO and SCLO outputs.

Reset

Reset should be applied for four system clock cycles. Reset will:

- Clear SSD
- Clear the command register but leave the bypass flag set.

After a reset has been applied the SAA7346 will start-up in bypass mode.

Kill interface

The kill interface can be used to deactivate the DAC. The kill input is passed directly to the $\overline{KILLOUT}$ output when the bypass flag in the command register is set. When the flag is not set $\overline{KILLOUT}$ is generated by the SAA7346. It is LOW after leaving bypass mode, a reset or a FIFO flush. It will be LOW until the first error free word is read from the FIFO. The kill input has no effect or function when the bypass flag is not set.

Read cycle divide (RCD2)

The RCD2 input enables the modes of operation shown in Table 6. When RCD2 is HIGH the DRAM-read requests are halved allowing I^2S output speeds to vary. The factor n is called the over-speed factor.

Table 6 SAA7346 I^2S output speeds.

RCD2	I^2S INPUT SPEED	I^2S OUTPUT SPEED	APPLICATION
LOW	CAV(1)	n = 1	CAV CDROM player with standard audio speed
LOW(2)	n = 1	n = 1	delay line feature
LOW	n = 2	n = 1	shock proof CD player
LOW	n = 4	n = 1	high data rate CDROM/CDI player with standard audio speed
HIGH	n = 2	n = ½	musicians feature
HIGH	n = 4	n = ½	musicians feature

Notes

1. CAV with n = 4 speed at outer edge of disc; n = 1.5 at inner edge of disc.
2. To build-up a delay, RCD2 should be made HIGH temporarily for twice the delay time.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	0	6.5	V
P_{max}	maximum power dissipation	–	500	mW
T_{stg}	storage temperature	–55	+125	°C
T_{amb}	operating ambient temperature	–40	+85	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	80	K/W

CHARACTERISTICS

V_{DD} = 3.3 to 5.5 V; V_{SS} = 0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		3.3	5.0	5.5	V
I_{DD}	supply current	V_{DD} = 5.0 V	–	12	–	mA
I_{DDb}	bypass supply current	V_{DD} = 5.0 V; bypass mode	–	4	–	mA
I_{DDq}	quiescent supply current		–	–	100	µA
Digital inputs						
INPUTS: WCI, SDI, CLKIN, OTD AND RCD2; NORMAL CMOS						
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
I_{LI}	input leakage current	V_I = 0 V to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INPUT CLKIN						
f_{clk}	system clock frequency		–	16.9344	–	MHz
t_H	system clock HIGH time		35	–	65	ns
t_r	system clock rise time	0.8 V to (V_{DD} – 0.8 V)	–	–	20	ns
t_f	system clock fall time	(V_{DD} – 0.8 V) to 0.8 V	–	–	20	ns
INPUTS: CFLG, KILL, CONFIG AND SILD; WITH PULL-UP						
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
R_{PU}	input pull-up resistance	V_I = 0 V	–	50	–	kΩ
C_I	input capacitance		–	–	10	pF
INPUT TMS; WITH PULL-DOWN						
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
R_{PD}	input pull-down resistance	$V_I = V_{DD}$	–	50	–	kΩ
C_I	input capacitance		–	–	10	pF
INPUTS: $\overline{\text{RESET}}$, SCLI AND SICL; SCHMITT-TRIGGER						
V_{thr}	switching threshold voltage rising		–	–	$0.8V_{DD}$	V
V_{thf}	switching threshold voltage falling		$0.2V_{DD}$	–	–	V
V_{hys}	hysteresis voltage		–	$0.33V_{DD}$	–	V
C_I	input capacitance		–	–	10	pF
INPUT $\overline{\text{RESET}}$						
t_{RW}	RESET pulse width; active LOW		236	–	–	ns
Digital outputs						
OUTPUTS: FILL, S_NSF, RSB AND SSD; PUSH-PULL						
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OL} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.8 V to (V_{DD} – 0.8 V); C_L = 50 pF	–	–	15	ns
t_f	output fall time	(V_{DD} – 0.8 V) to 0.8 V; C_L = 50 pF	–	–	15	ns
OUTPUTS: SDO, SCLO, WCO, $\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, A0 TO A9; SLEW RATE PUSH-PULL						
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OL} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.8 V to (V_{DD} – 0.8 V); C_L = 50 pF	–	–	20	ns
t_f	output fall time	(V_{DD} – 0.8 V) to 0.8 V; C_L = 50 pF	–	–	20	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
OUTPUT $\overline{\text{KILLOUT}}$; OPEN DRAIN						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.4	V
I_O	output current		–	–	2	mA
C_L	load capacitance		–	–	50	pF
t_f	output fall time	(V_{DD} – 0.8 V) to 0.8 V; C_L = 50 pF	–	–	30	ns
INPUTS/OUTPUTS: D0 TO D3; NORMAL CMOS WITH SLEW RATE CONTROLLED PUSH-PULL						
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
I_{LI}	input leakage current	V_I = 0 V to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OL} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.8 V to (V_{DD} – 0.8 V); C_L = 50 pF	–	–	20	ns
t_f	output fall time	(V_{DD} – 0.8 V) to 0.8 V; C_L = 50 pF	–	–	20	ns
INPUT/OUTPUT SIDA; NORMAL CMOS WITH PUSH-PULL						
V_{IL}	LOW level input voltage		–0.3	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
I_{LI}	input leakage current	V_I = 0 V to V_{DD}	–10	–	+10	µA
C_I	input capacitance		–	–	10	pF
V_{OL}	LOW level output voltage	I_{OL} = 4 mA	0	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OL} = –4 mA	V_{DD} – 0.4	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	0.8 V to (V_{DD} – 0.8 V); C_L = 50 pF	–	–	15	ns
t_f	output fall time	(V_{DD} – 0.8 V) to 0.8 V; C_L = 50 pF	–	–	15	ns
I²S timing						
RECEIVER (SEE FIG.9)						
Clock input SCLI						
T_{cy}	clock cycle time		118.1[1]	236.2[2]	472.4[3]	ns
t_H	clock HIGH time		41.3[1]	–	–	ns
t_L	clock LOW time		41.3[1]	–	–	ns
Inputs: SDI and WCI						
t_{su}	set-up time		23.6	–	–	ns
t_h	hold time		10	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TRANSMITTER (SEE FIG.8)						
Clock output SCLO						
T_{cy}	clock cycle time		–	472.4[3]	944.8[4]	ns
t_H	clock HIGH time		165.3	–	–	ns
t_L	clock LOW time		165.3	–	–	ns
Outputs: SDO and WCO						
t_d	delay time		–	–	377	ns
t_h	hold time		40	–	–	ns
Microcontroller interface timing (see Figs 12 and 13)						
INPUTS: SICL AND SILD						
t_H	input HIGH time		180	–	–	ns
t_L	input LOW time		180	–	–	ns
t_r	rise time	0.8 V to (V_{DD} – 0.8 V)	–	–	240	ns
t_f	fall time	(V_{DD} – 0.8 V) to 0.8 V	–	–	240	ns
Read mode (see Fig.12)						
t_d	delay time SILD to SIDA valid		120	–	–	ns
t_{pd}	propagation delay time SICL to SIDA		–	–	110	ns
Write mode (see Fig.13)						
t_{su1}	set-up time SIDA to SICL		40	–	–	ns
t_h	hold time SICL to SIDA		–	–	180	ns
t_{su2}	set-up time SICL to SILD		180	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DRAM interface timing (see Figs 14 and 15)						
T_{cy}	read or write cycle time		160	–	–	ns
t_{CAC}	access time from $\overline{CAS}$		–	–	20	ns
t_{OAC}	access time from $\overline{OE}$		–	–	20	ns
t_{h3}	$\overline{OE}$ to data input hold time		0	–	–	ns
t_{RH}	$\overline{RAS}$ HIGH time		70	–	–	ns
t_{RL}	$\overline{RAS}$ LOW time		80	–	10000	ns
t_{h1}	$\overline{RAS}$ hold time		20	–	–	ns
t_{h2}	$\overline{RAS}$ hold time to $\overline{OE}$ LOW		20	–	–	ns
t_{CL}	$\overline{CAS}$ LOW time		20	–	10000	ns
t_{h4}	$\overline{CAS}$ hold time		80	–	–	ns
t_{CRd}	delay time from $\overline{CAS}$ HIGH to $\overline{RAS}$		10	–	–	ns
t_{RCd}	delay time from $\overline{RAS}$ to $\overline{CAS}$		25	–	–	ns
t_{Rd}	$\overline{RAS}$ to column address delay time		20	–	–	ns
t_{su1}	row address set-up time		0	–	–	ns
t_{RAh}	row address hold time		15	–	–	ns
t_{su2}	column address set-up time		0	–	–	ns
t_{CAh}	column address hold time		20	–	–	ns
t_{Rh}	column address hold time from $\overline{RAS}$ LOW		60	–	–	ns
t_{l}	column address to $\overline{RAS}$ lead time		40	–	–	ns
t_{RCh}	read command hold time		0	–	–	ns
t_{RRh}	read command hold time to $\overline{RAS}$		12	–	–	ns
t_{Wsu}	write command set-up time		0	–	–	ns
t_{Wh1}	write command hold time		15	–	–	ns
t_{WL}	write command LOW time		15	–	–	ns
t_{Wh2}	write command hold time from $\overline{RAS}$		60	–	–	ns
t_{WCl}	write command to $\overline{CAS}$ lead time		20	–	–	ns
t_{WRl}	write command to $\overline{RAS}$ lead time		20	–	–	ns
t_{Dsu}	data output set-up time		0	–	–	ns
t_{Dh}	data output hold time		15	–	–	ns
t_{DRh}	data output hold time from $\overline{RAS}$		60	–	–	ns

Notes

1. n = 4.
2. n = 2.
3. n = 1.
4. n = ½.

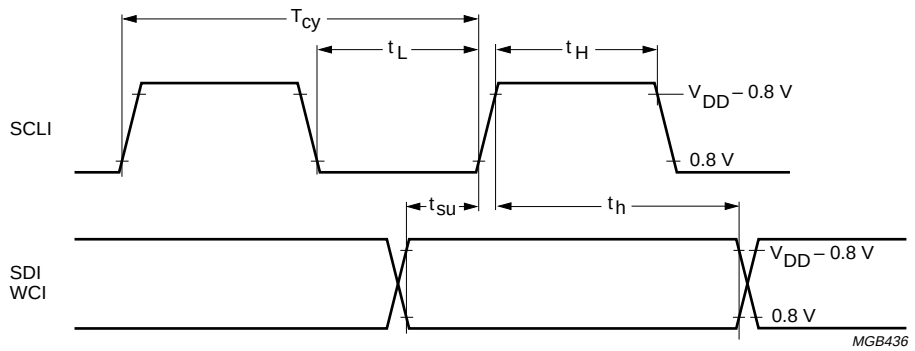


Fig.8 I^2S input timing.

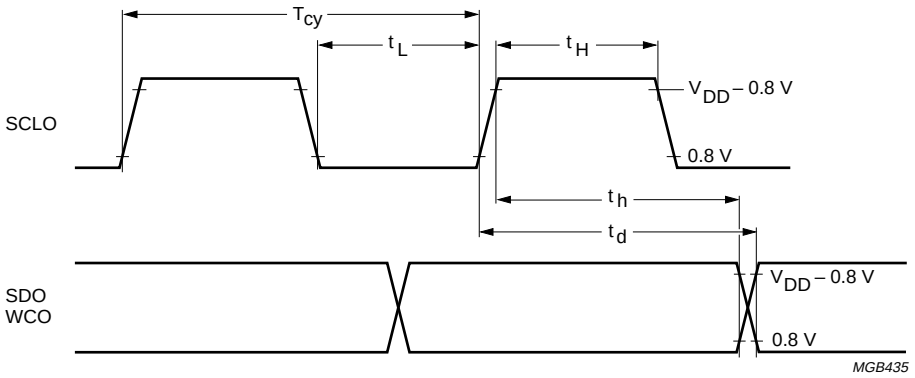


Fig.9 I^2S output timing.

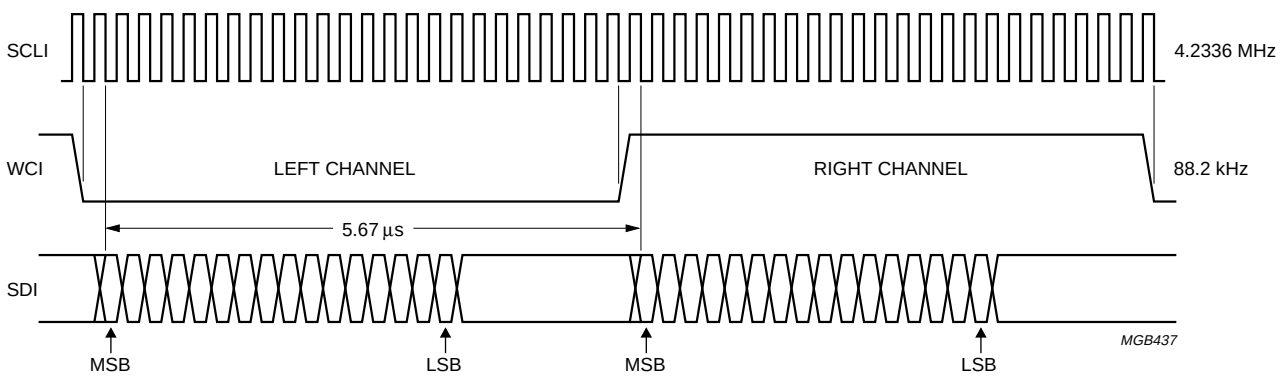


Fig.10 Typical I^2S data input waveform; f = 4.2 MHz; n = 2.

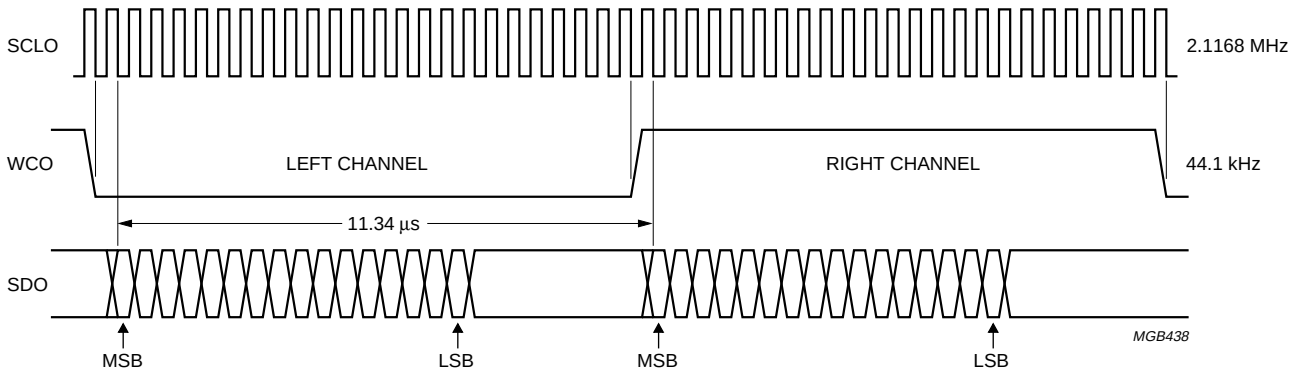


Fig.11 Typical I²S data output waveform; f = 2.1 MHz; n = 1.

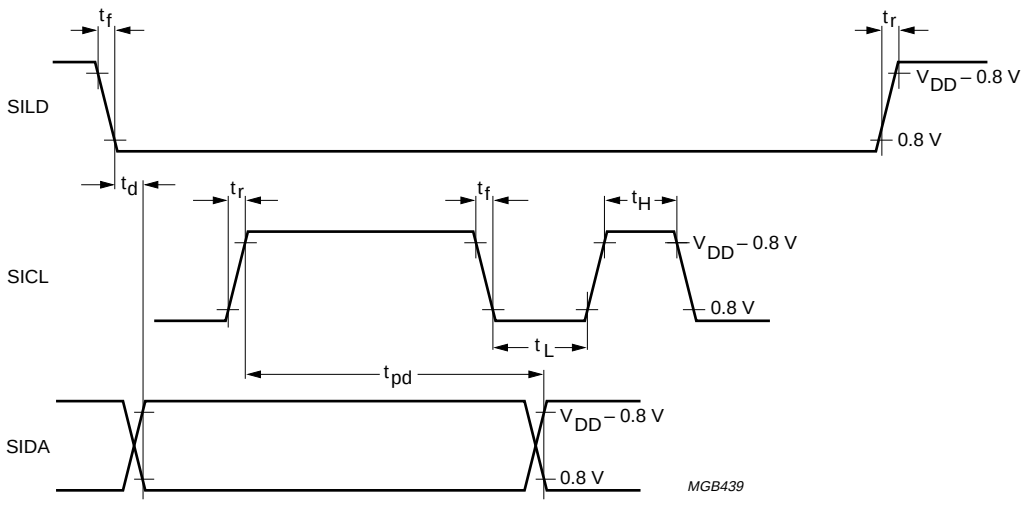


Fig.12 Microcontroller timing; READ mode.

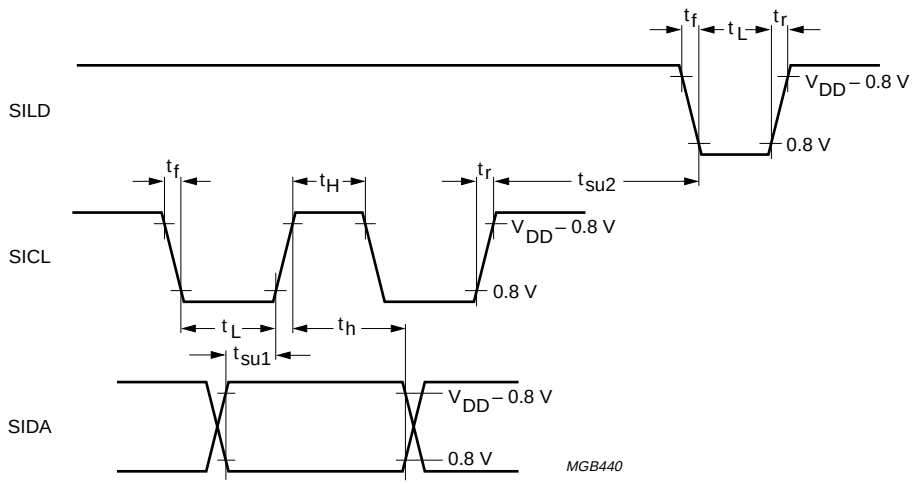


Fig.13 Microcontroller timing; WRITE mode.

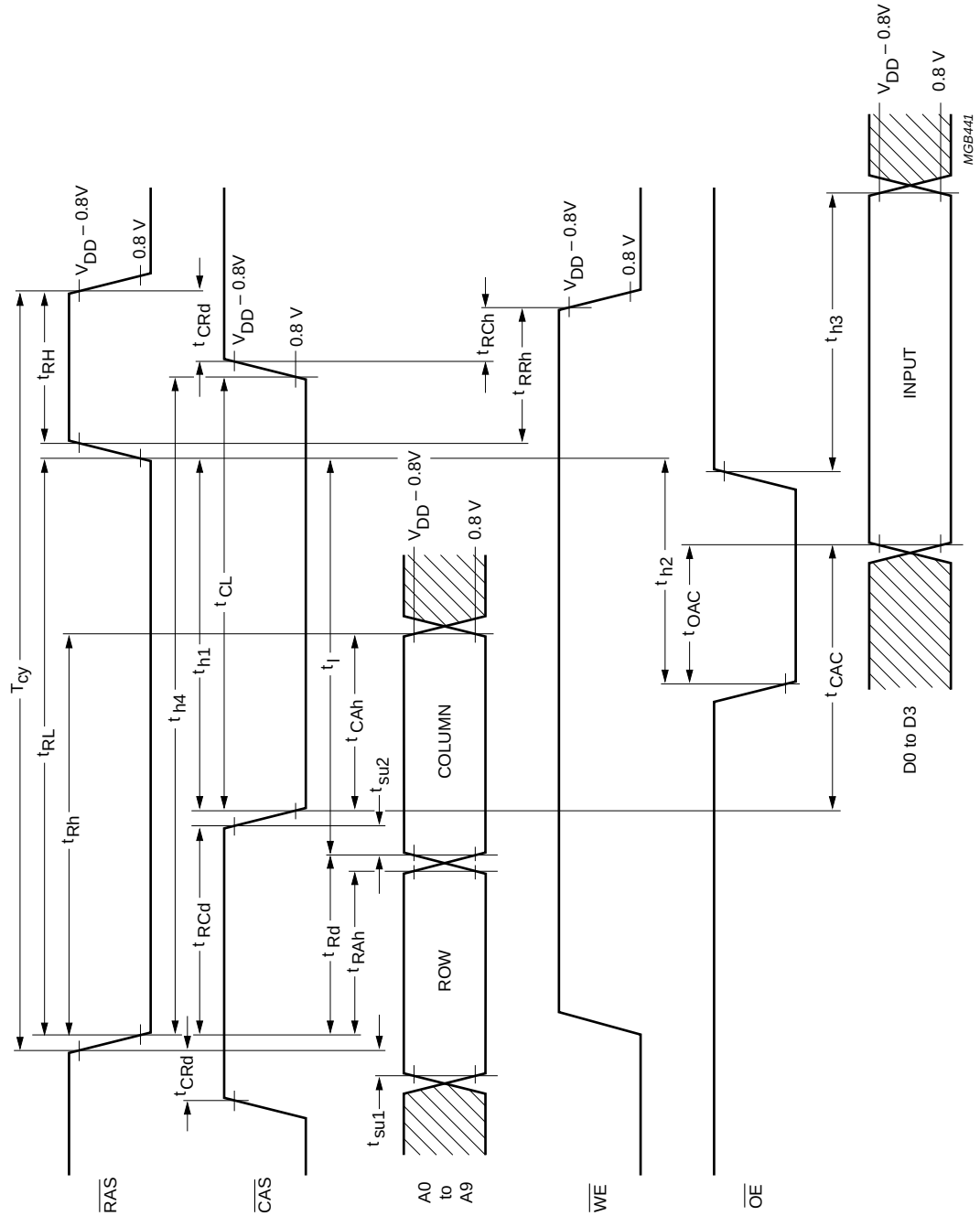


Fig.14 READ cycle timing.

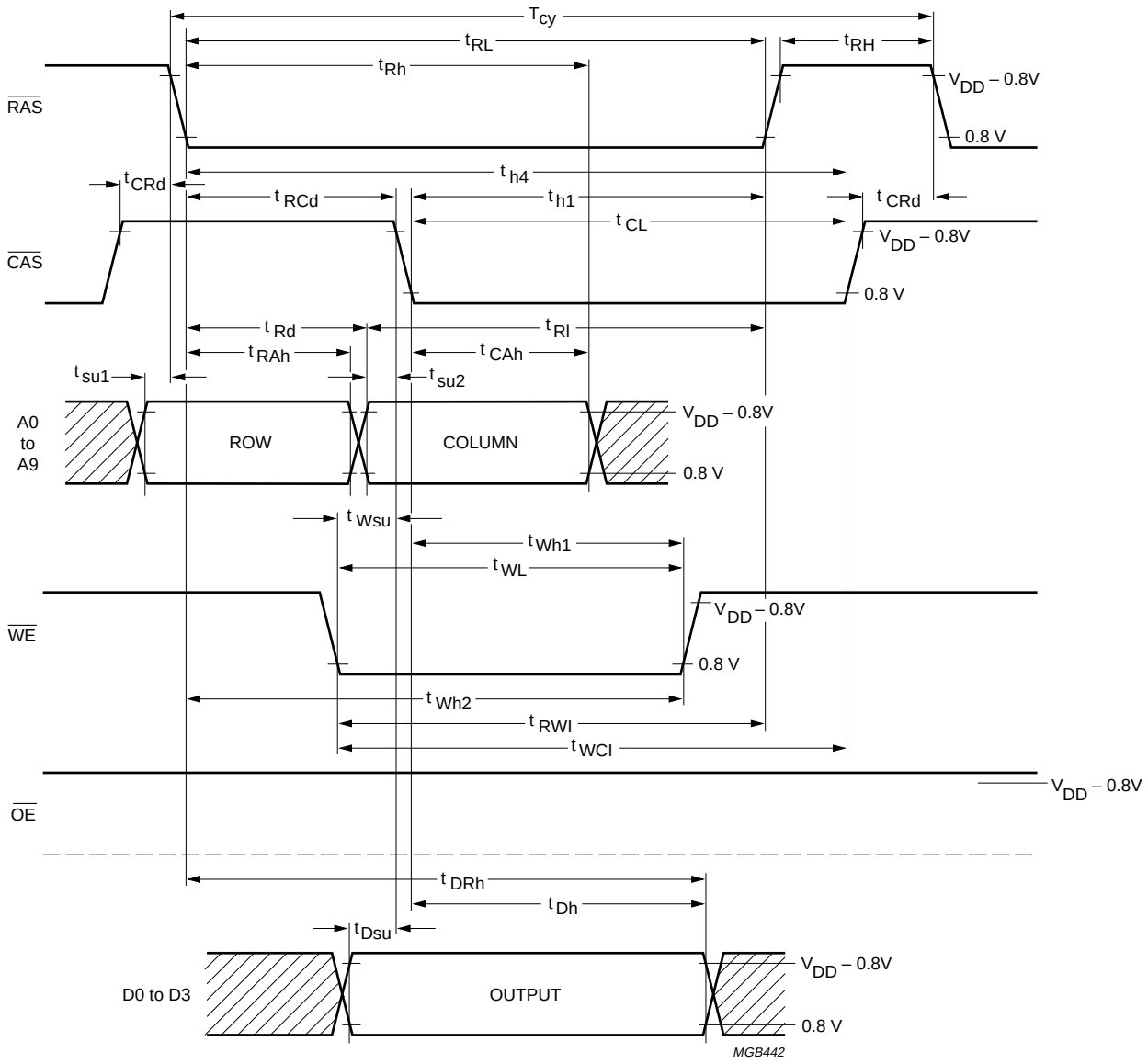


Fig.15 WRITE cycle timing.

APPLICATION INFORMATION

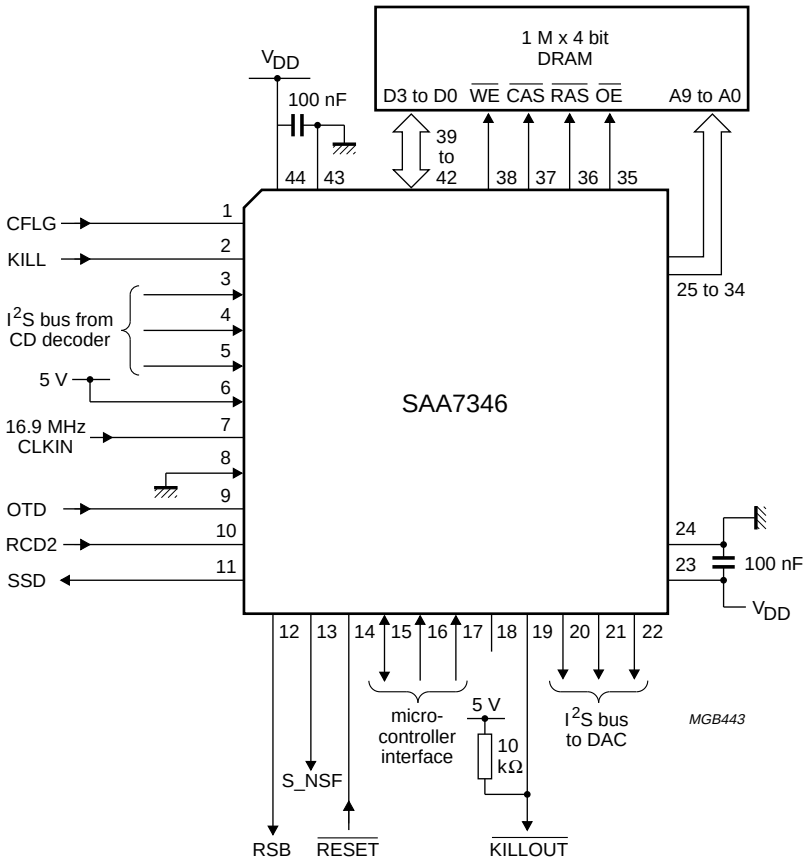
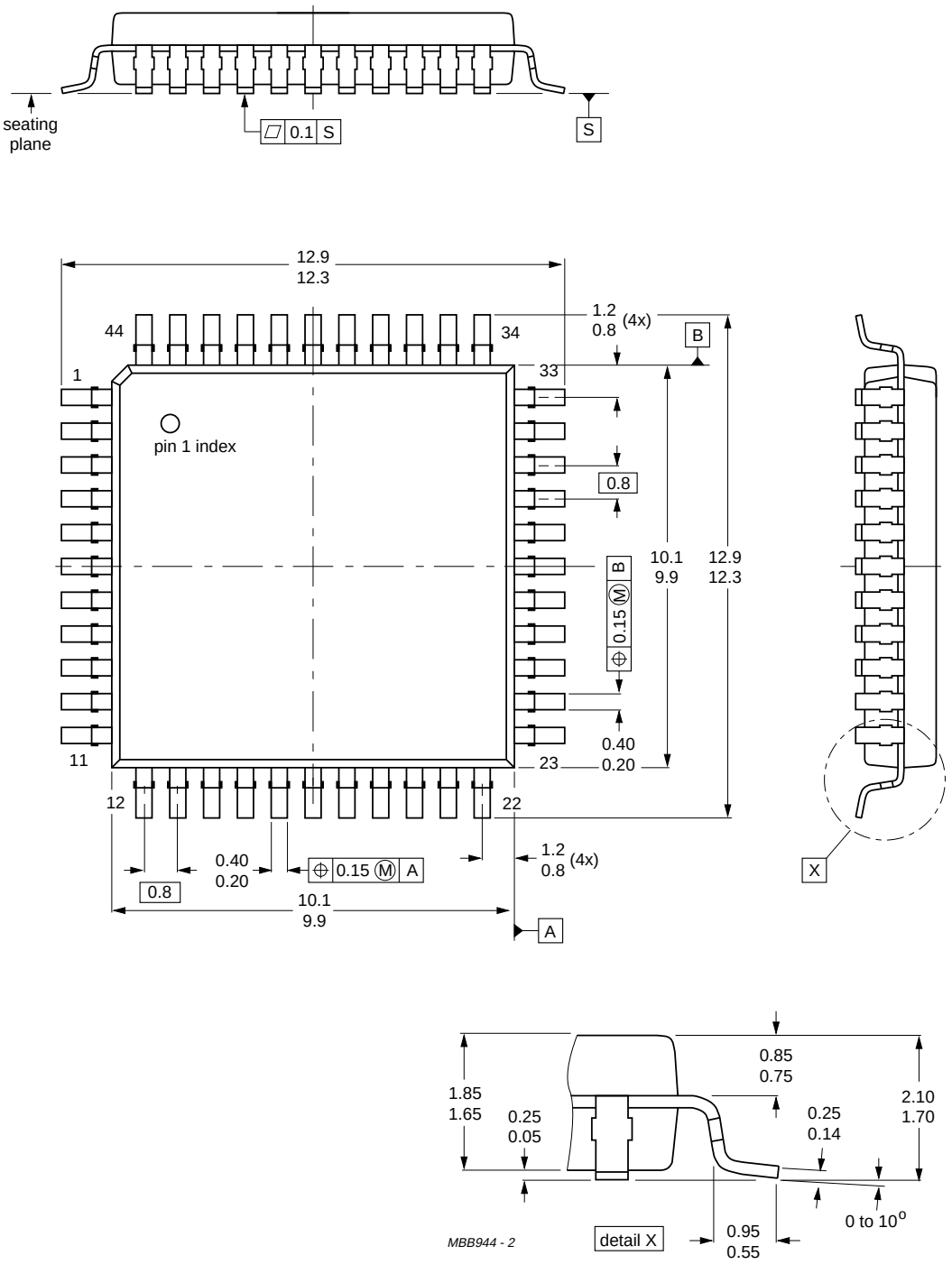


Fig.16 SAA7346 application diagram.

PACKAGE OUTLINE



Dimensions in mm.

Fig.17 Plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm; (SOT307-2; QFP44).

SOLDERING

Plastic quad flat-packs

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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